Dragonchip

DCT-EDP Rev3.x User Manual

Document Revision 1.3

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1 Introduction

This document aims at describing the operation of the tool ‘DCT-EDP Rev3.x’. DCT-EDP is primarily used for flash programming and debugging software running on 8051-based System-on-Chip (SoC) devices from Dragonchip.

1.1 Box Contents

1. 1 x DCT-EDP Rev3.x
2. 1 x USB cable
3. 1 x 20-pin flat cable with 2x10 2.54mm connector
4. 1 x 6-pin flat cable with 1x6 2.54 connector

1.2 Useful links

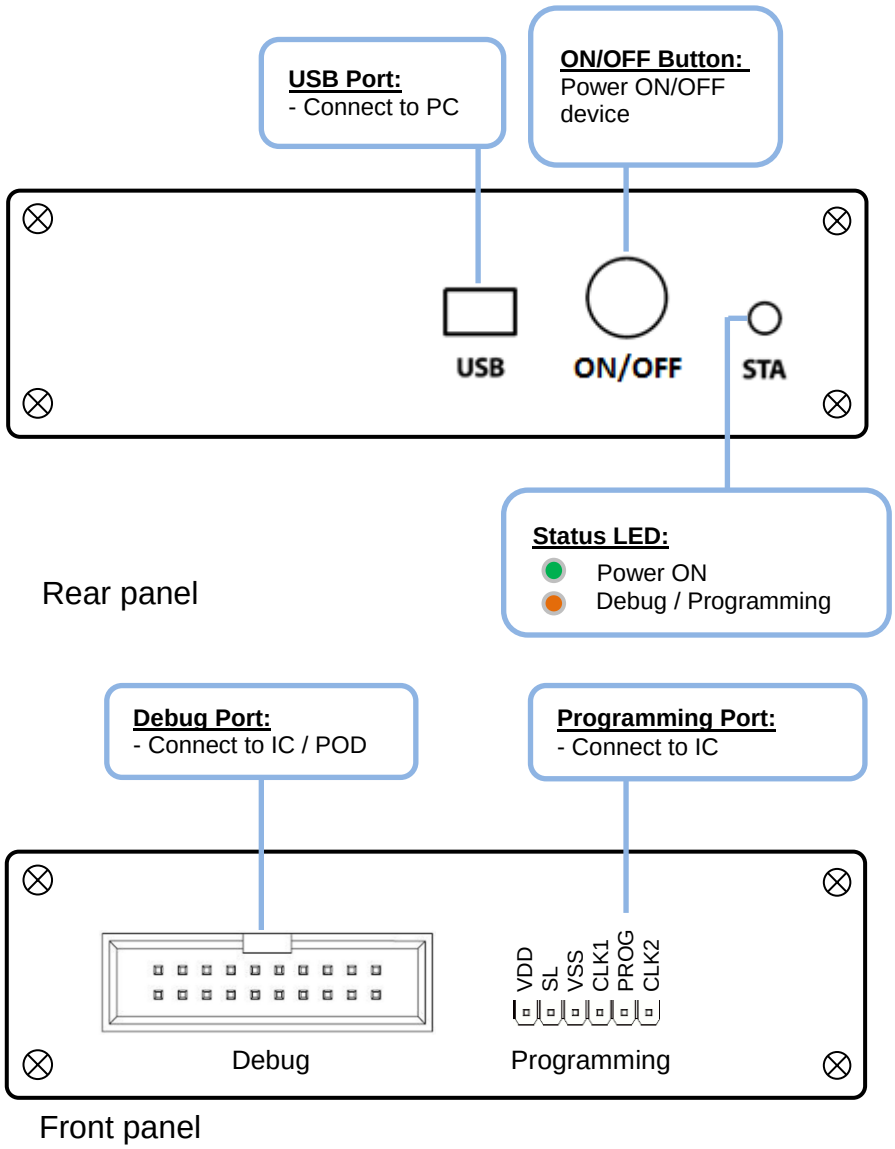
Generally, all the products information is available in our website. Below are some examples.

1. DC6688
    1. Emulator – download latest software installer(Software SLP, Emulator driver, and Source Code Template in one package) and user manual
    2. Technical website

2. DC6288
    1. Emulator – download latest software installer(Software SLP, Emulator driver, and Source Code Template in one package) and user manual
    2. Technical website

2 Hardware

2.1 Control Interface



Front panel have two ports:

1. Debug port
   甲、Keil use this port for debug and programming
2. Programming port
   甲、Software SLP use this port for programming

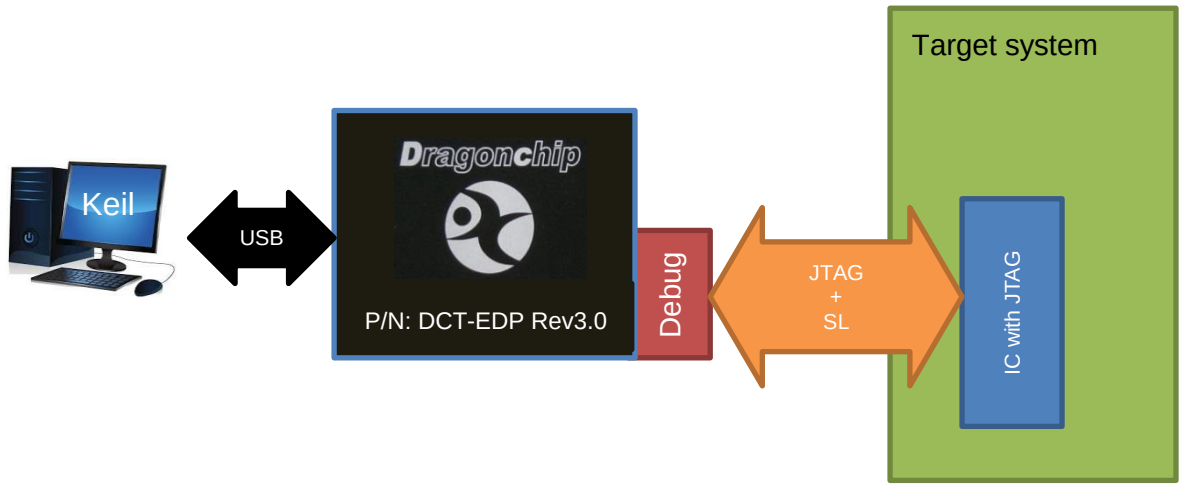
3 Debug

3.1 Hardware setup

Debug port provides JTAG and SL interface to IC package with JTAG and SL pins. Prior to entering debug mode in Keil IDE, the firmware will be downloaded automatically through this SL interface. JTAG interface is used for debug communication.

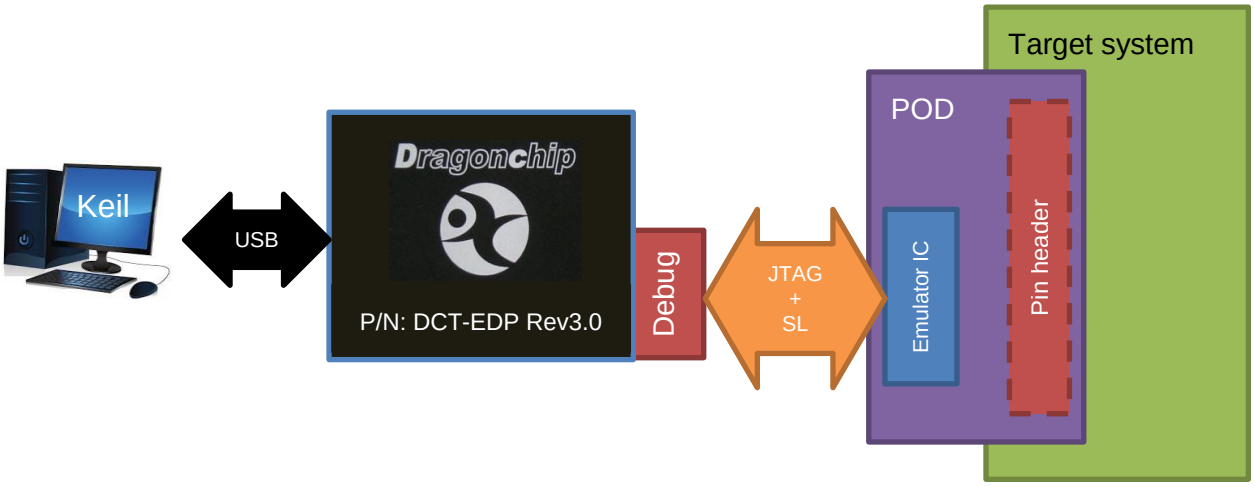
There are two cases of connection depending on whether the package provided with JTAG pins or not.

1. IC package with JTAG pins



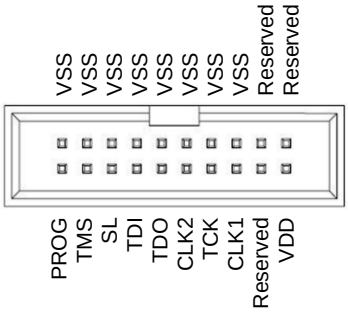
An example is DC6288FT32N3E. In this case, the debug port can connect directly to the IC.

2. IC package without JTAG pins



An example is DC6688FL96TT, TSSOP28 without JTAG pin. The DCT-EDP has to connect to target system through a POD board.

3.2 Debug port pin assignment



Reserved pins must be no connection.
VDD pin, with maximum output current 500mA, should be handled with care to avoid conflict with the power from self-powered target system. They should not be connected together unless target system power supplied by VDD pin of Debug port. If the power of Dragonchip IC is supplied by self-powered target system, VDD pin of Debug port should be left disconnected.

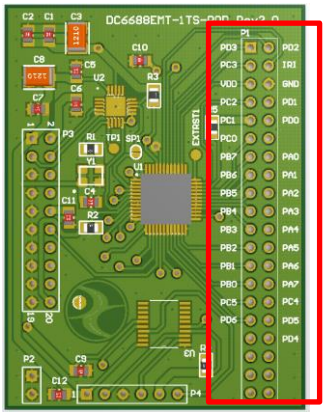
The following series are compulsory to connect VDD pin of Debug port, instead of target system.
1. DC6688
2. DC6388

Ribbon cable is strongly recommended for better noise immunity.

3.3 Pin assignment on POD board

3.3.1 DC6688EMT-1TS-POD Rev2.0 board

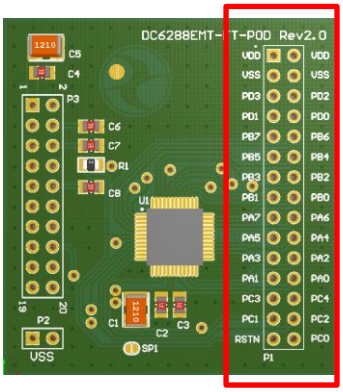
This board can support both DC6688FST and DC6688FLT for those packages without JTAG pins.



Pin	Description	Pin	Description
1	PD3	2	PD2
3	PC3	4	IRI
5	VDD(3.3V)	6	VSS
7	PC2	8	PD1
9	PC1	10	PD0
11	PC0	12	NC
13	PB7	14	PA0
15	PB6	16	PA1
17	PB5	18	PA2
19	PB4	20	PA3
21	PB3	22	PA4
23	PB2	24	PA5
25	PB1	26	PA6
27	PB0	28	PA7
29	PC5	30	PC4
31	PD6	32	PD5
33	NC	34	PD4
35	NC	36	NC
37	NC	38	NC
39	NC	40	NC

3.3.2 DC6288EMT-FT-POD Rev2.0 board

This board can support both DC6288FT for those packages without JTAG pins.



Pin	Description	Pin	Description
1	VDD(3.3V)	2	VDD(3.3V)
3	VSS	4	VSS
5	PD3	6	PD2
7	PD1	8	PD0
9	PB7	10	PB6
11	PB5	12	PB4
13	PB3	14	PB2
15	PB1	16	PB0
17	PA7	18	PA6
19	PA5	20	PA4
21	PA3	22	PA2
23	PA1	24	PA0
25	PC3	26	PC4
27	PC1	28	PC2
29	NC	30	PC0

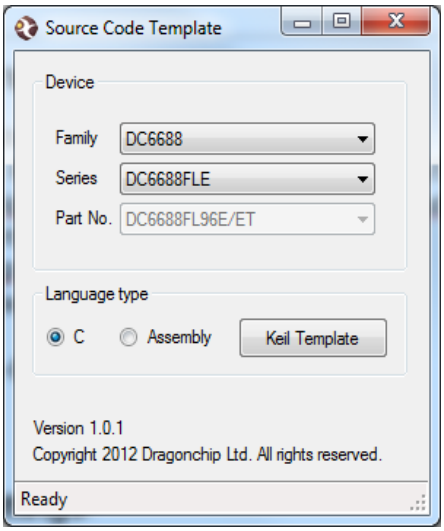
3.4 Software Installation

Install the following components in order:

1) Keil PK51 Prof. Developers Kit (recommend v9.55)
   It must be installed prior to the following components.
2) Dragonchip 'DC_TOOL_Rev3.2.1.exe' or higher which includes the following items:
   a. Source Code Template
   b. Emulator Driver
   c. Software SLP

3.4.1 Source Code Template

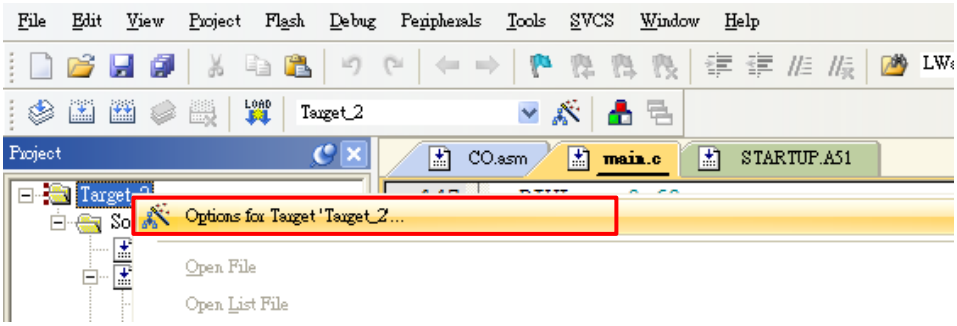
This useful tool can help to generate Keil Project Templates for various Dragonchip 8051-based MCU products with all necessary project settings for using emulators. User can either start the development with the generated source code template or compare the project settings with their existing Keil project.



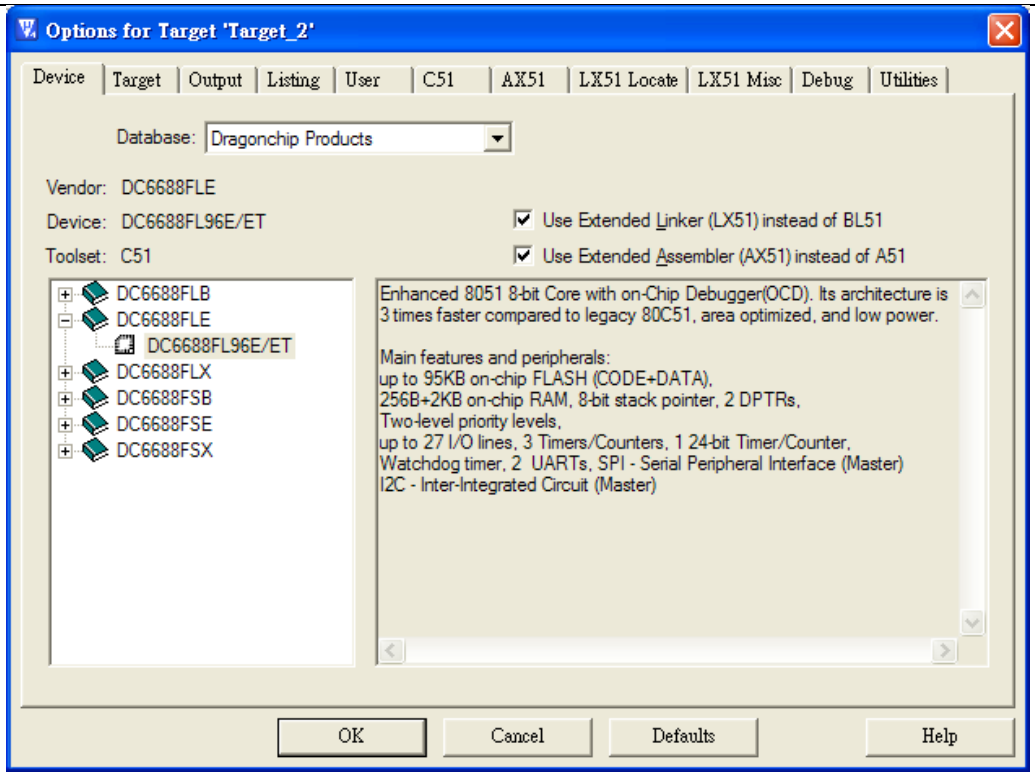
3.4.2 Keil Project Settings

All necessary Keil Project Settings are listed in this section. The settings might vary from one part no. to another.
For illustration, DC6688FL96E is taken as an example.

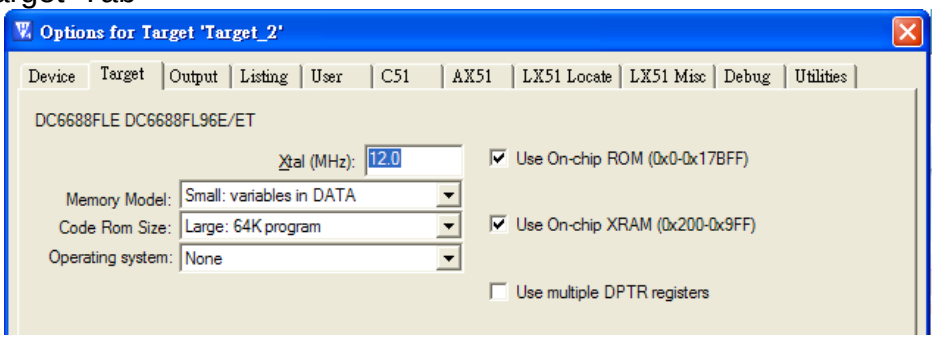
1) Enter 'Options for Target'



2) 'Device' Tab - Select DC6688 part from the list.

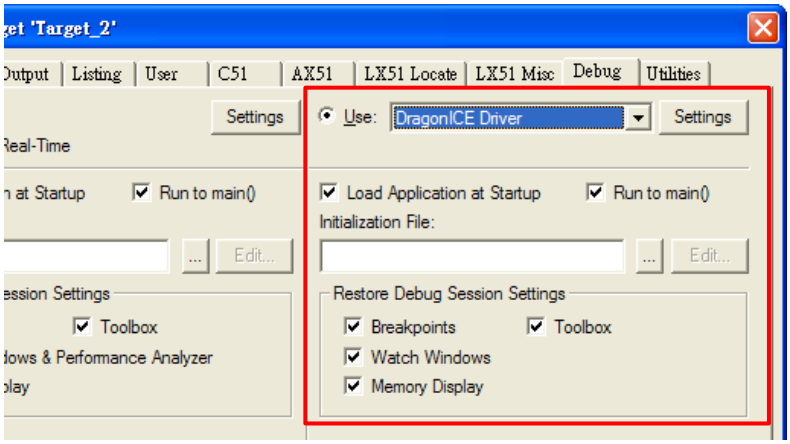


3) ‘Target’ Tab

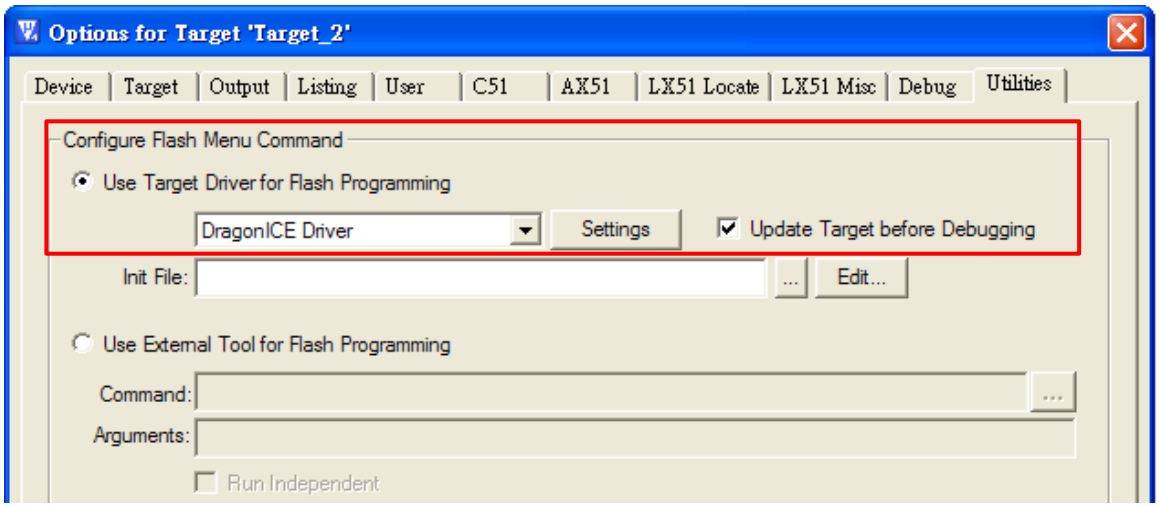


Note: The Clock frequency in this page is invalid setting. The setting should be selected in ‘Programming Setting’ instead.

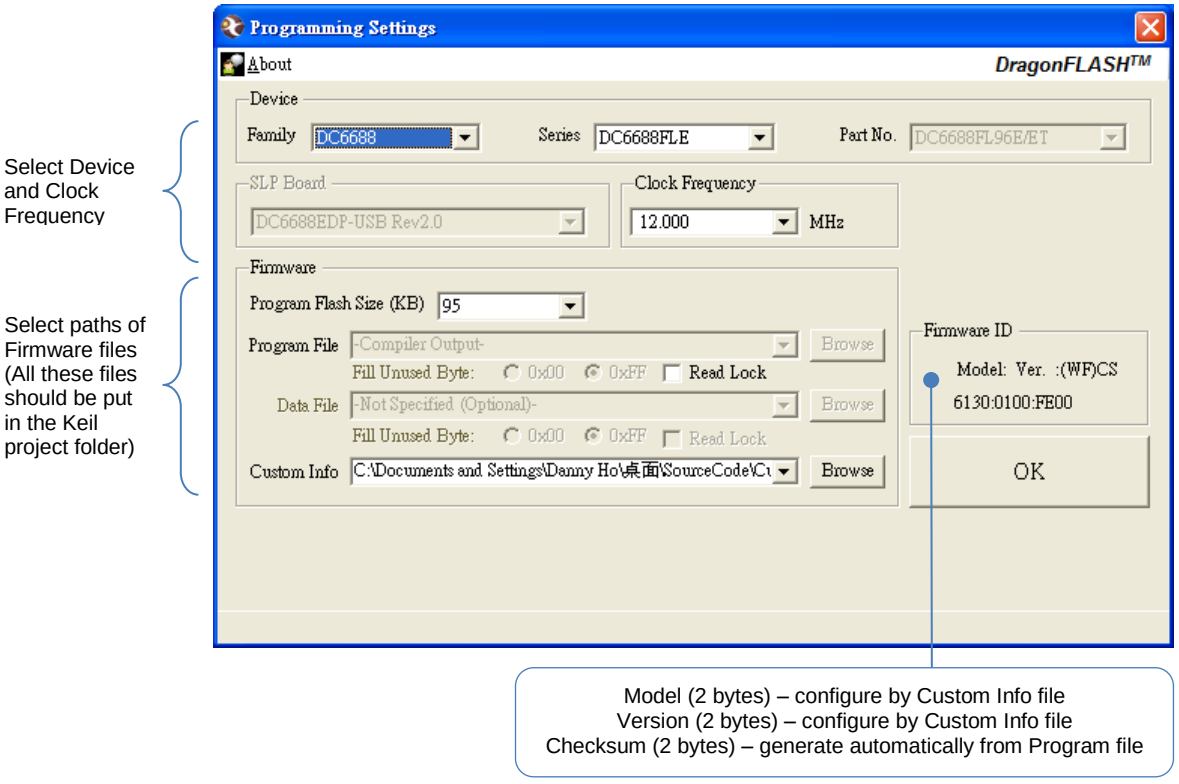
4) ‘Debug’ Tab - Follow the settings shown below:



5) ‘Utilities’ Tab - Follow the settings shown below:



6) Click ‘Settings’ in ‘Utilities’ tab to enter Programming Setting. Input relevant settings for programming the emulator chip.



Note: Program File does not need to select path.

3.5 View Memory Content

3.5.1 DC6688F2SER/F2STR

Memory	Size	Memory Type	Start Address	End Address	Example
Program Flash	Up to 2000B	code	0x0000	0x07CF	C:0x00000
EEPROM	16 bytes	xdata	0x100	0x10F	X:0x0100
Internal SRAM	64 bytes	idata	0x00	0x3F	I:0x00
SFR	128 bytes	data	0x80	0xFF	D:0x80
XFR	256 bytes	xdata	0x00	0xFF	X:0x0000

3.5.2 DC6688FLB

Memory	Size	Memory Type	Start Address	End Address	Example
Program Flash					
FL16B	Up to 12KB	code	0x0000	0x2FFF	C:0x0000
FL32B	Up to 24KB	code	0x0000	0x5FFF	C:0x0000
Data Flash					
FL16B	4KB	code	0x6000	0x6FFF	C:0x6FFF
FL32B	8KB	code	0x6000	0x7FFF	C:0x6000
Internal SRAM	256 bytes	idata	0x00	0xFF	I:0x00
Expanded SRAM	2KB	xdata	0x0200	0x09FF	X:0x0200
SFR	128 bytes	data	0x80	0xFF	D:0x80
XFR	256 bytes	xdata	0x00	0xFF	X:0x0000

3.5.3 DC6688FLX/FLE/FLT/FL96TE

Memory	Size	Memory Type	Start Address	End Address	Example
Program/Data Flash					
FL32T	Up to 31KB			0x7BFF	
FLX/FL64T	Up to 64KB	code	0x0000	0xFFFF	C:0x0000
FLE/FL96T	Up to 95KB			0x17BFF	
FL96TE	Up to 95KB			0x17BFF	
Internal SRAM	256 bytes	idata	0x00	0xFF	I:0x00
Expanded SRAM					
FLX/FLE	2KB		0x0200	0x09FF	X:0x0200
FL32T	1.5KB	xdata	0x0200	0x07FF	X:0x0200
FL64T/FL96T	3KB		0x8200	0x8DFF	X:0x8200
FL96TE	3KB		0x8200	0x8DFF	X:0x8200
SFR	128 bytes	data	0x80	0xFF	D:0x80
XFR	256 bytes	xdata	0x00	0xFF	X:0x0000

3.5.4 DC6688FSB/FSX/FSE/FST

Memory	Size	Memory Type	Start Address	End Address	Example
Program Flash FSB FST FSX/FSE	 Up to 30KB Up to 29.5KB Up to 62KB	code	0x0000	 0x77FF 0x75FF 0xF7FF	C:0x0000
EEPROM	64 bytes	xdata	0x100	0x13F	X:0x0100
Internal SRAM	256 bytes	idata	0x00	0xFF	I:0x00
SFR	128 bytes	data	0x80	0xFF	D:0x80
XFR	256 bytes	xdata	0x00	0xFF	X:0x0000

3.5.5 DC6688BT

Memory	Size	Memory Type	Start Address	End Address	Example
Program/Data Flash BT32 BT96	 Up to 31KB Up to 95KB	code	0x0000	 0x7BFF 0x17BFF	C:0x0000
Internal SRAM	256 bytes	idata	0x00	0xFF	I:0x00
Expanded SRAM BT32 BT96	 1.5KB 3KB	xdata	 0x0200 0x8200	 0x07FF 0x8DFF	 X:0x0200 X:0x8200
SFR	128 bytes	data	0x80	0xFF	D:0x80
XFR	256 bytes	xdata	0x00	0xFF	X:0x0000

3.5.6 DC6288FT

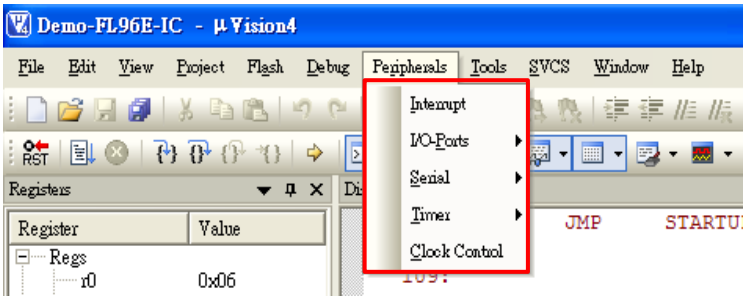
Memory	Size	Memory Type	Start Address	End Address	Example
Program/ Data Flash	Up to 31KB	code	0x00000	0x7BFF	C:0x00000
Internal SRAM	256 bytes	idata	0x00	0xFF	I:0x00
Expanded SRAM	1KB	xdata	0x0200	0x05FF	X:0x0200
	1.5KB	xdata	0x0200	0x07FF	X:0x0200
	2KB	xdata	0x0200	0x09FF	X:0x0200
SFR	128 bytes	data	0x80	0xFF	D:0x80
XFR	256 bytes	xdata	0x00	0xFF	X:0x0000

3.6 Supplementary Information

3.6.1 Limitation

A) Keil IDE

DragonICE does not support the following features.



B) Hardware

1) Voltage Supply

甲、The VDD of Debug port is fixed at specified voltage listed below. User should only do emulation at this voltage level.

Items	VDD/V
DC6288	3.3
DC6388	3.3
DC6688	3.3
DC6688FL32TC	1.8

2) Peripherals

甲、When the emulator is stopped in debugging platform, all the running peripherals (e.g. timer 2) will still keep running. Hence, the peripherals will be out of synchronization with the code instruction.

3) Counter A in one shot mode

甲、In one shot mode (CAM = 0), this bit have to reset to 0 every time before setting CAS = 1.

3.6.2 Troubeshooting

1) Driver Installation

After installing the DragonICE driver, plug the emulator to PC, the driver will be installed automatically for port connected. In case the PC fails to locate the driver, select the driver path “C:\WINDOWS\system32” manually.

2) Upgrade Keil Project

When uv2/ uv3 projects are closed, user can choose to upgrade the project to an uv4 project (*.uvproj).

3) Complie Keil Project

Always compile the code before entering the Keil debugging environment. Otherwise the emulated flash content may not be updated and the debug action may not match with the displayed code.

For example,

a) Cursor jumped to a wrong code location in debugger.

b) ‘Step’ instruction wrong executed as ‘Free Run’ instruction.

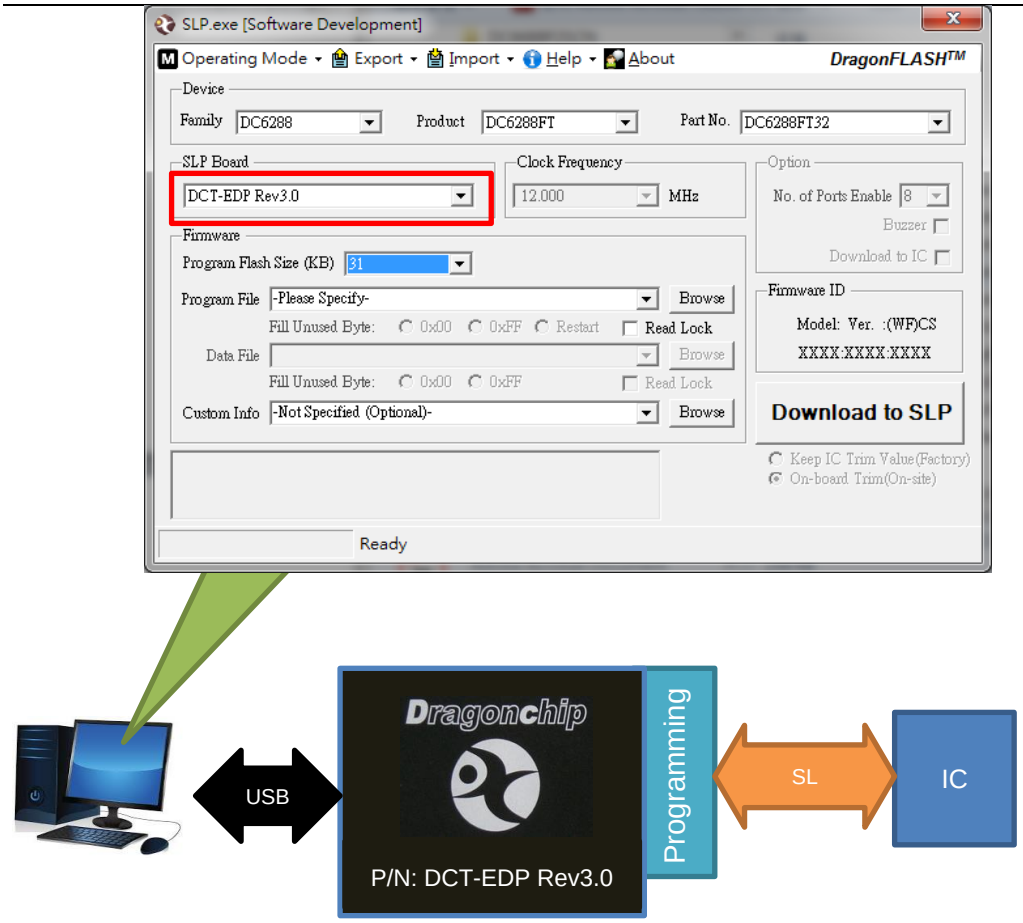
4 Programming

4.1 Software Installation

Software SLP is required on PC to control the hardware. Detail refers to section 3.4.

4.2 Hardware setup

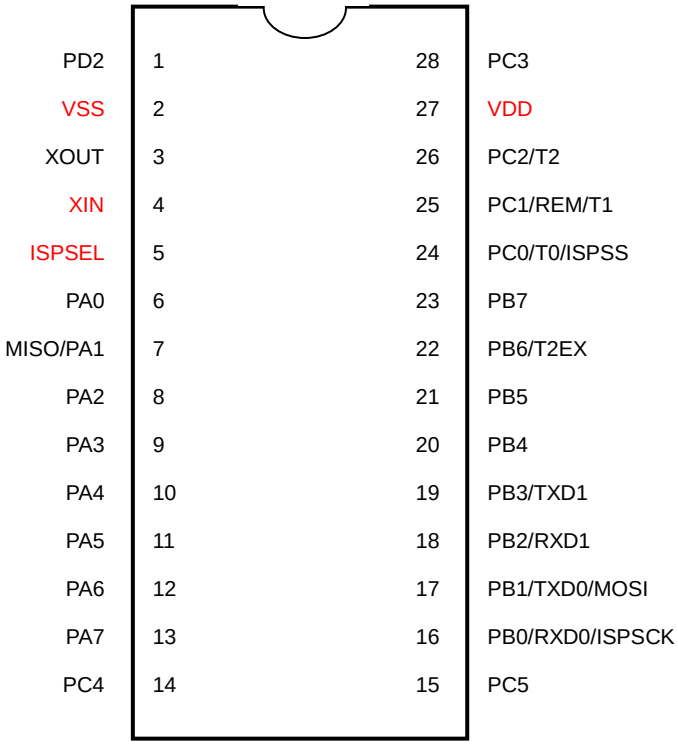
Programming port provides SL interface to IC. Software SLP will automatically select this programming port to download firmware to IC.
During debug, this port is disabled automatically.
Warning: Keil IDE must exit debugger mode before using this port via Software SLP.



Detail of Software SLP operation can refer to SLP user manual.

4.3 DC6688FSX

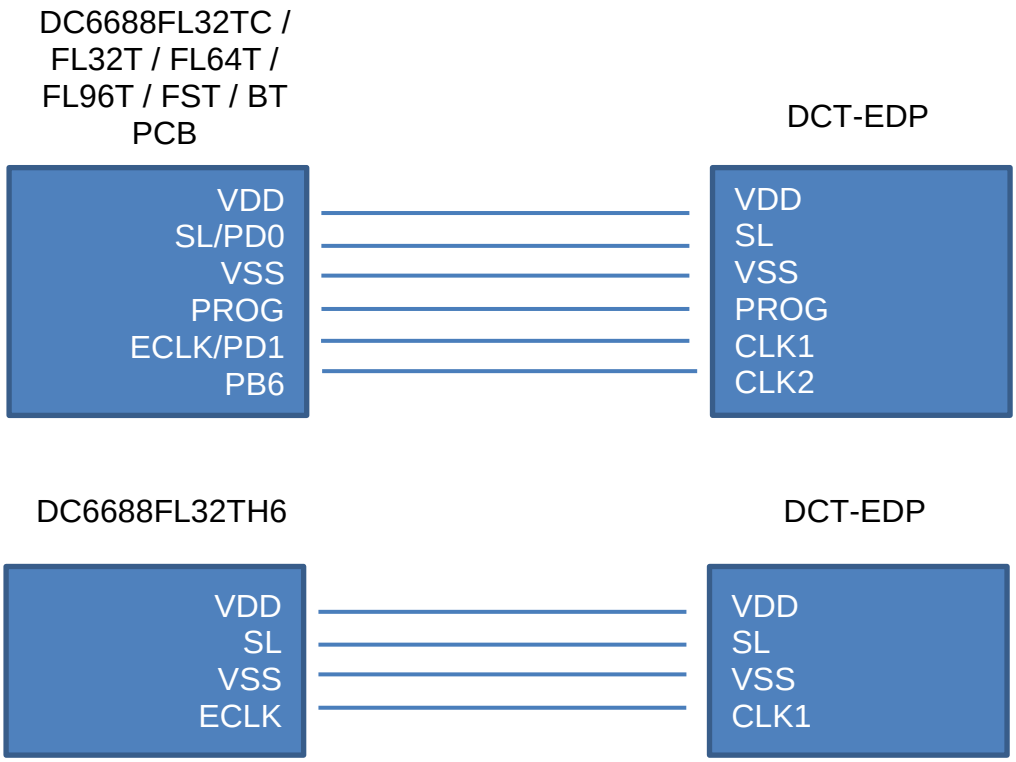
The 4-pin connection to the DCT-EDP's programming port from chip is shown below. 3-pin connection is not supported.



4MHz of clock frequency on Software SLP below must be selected if the board resonator is 12MHz.

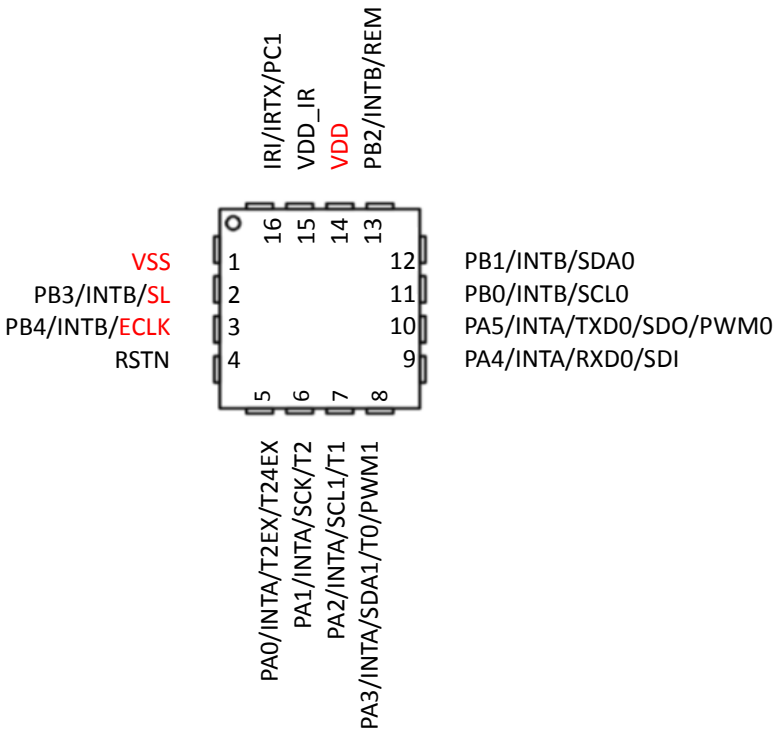
4.4 DC6688FST/FLT/BT

To do trimming during programming stage, 6 pads are required on PCB to complete this process.

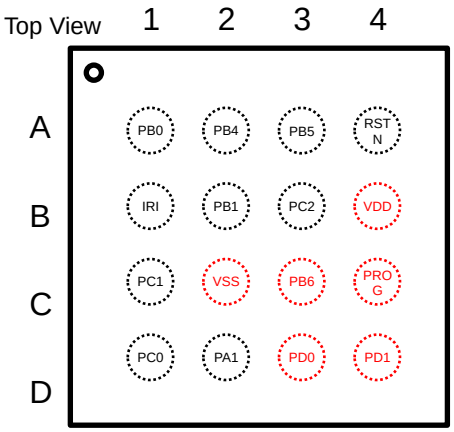


DC6688FL32TH6 only requires 4 pads.

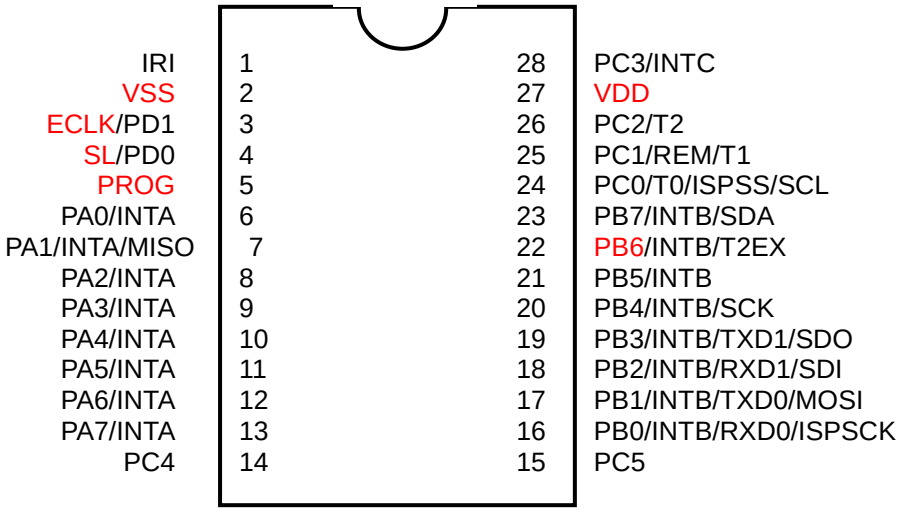
DC6688FL32TH6 (QFN16)



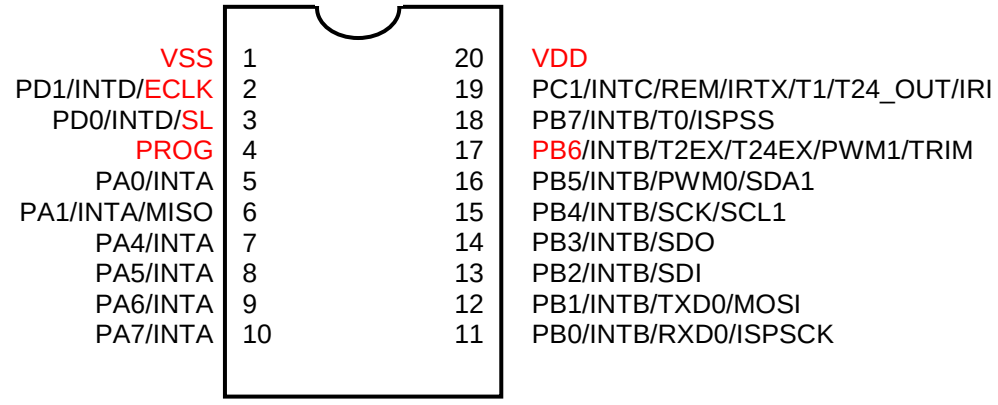
DC6688FL32TC



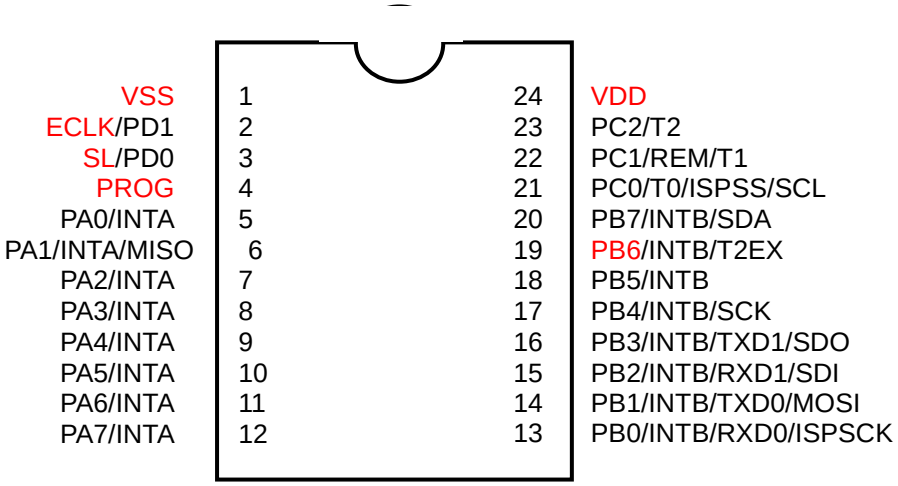
DC6688FL32TT / FL96TT



DC6688FL32TH / FL64TH / FL96TH

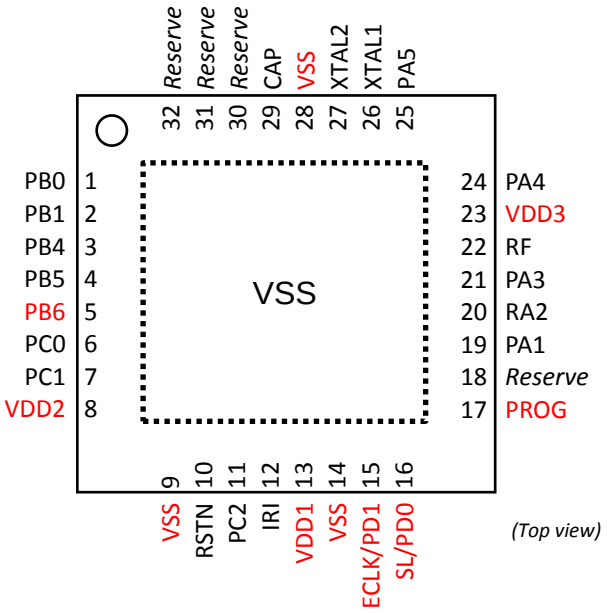


DC6688FST



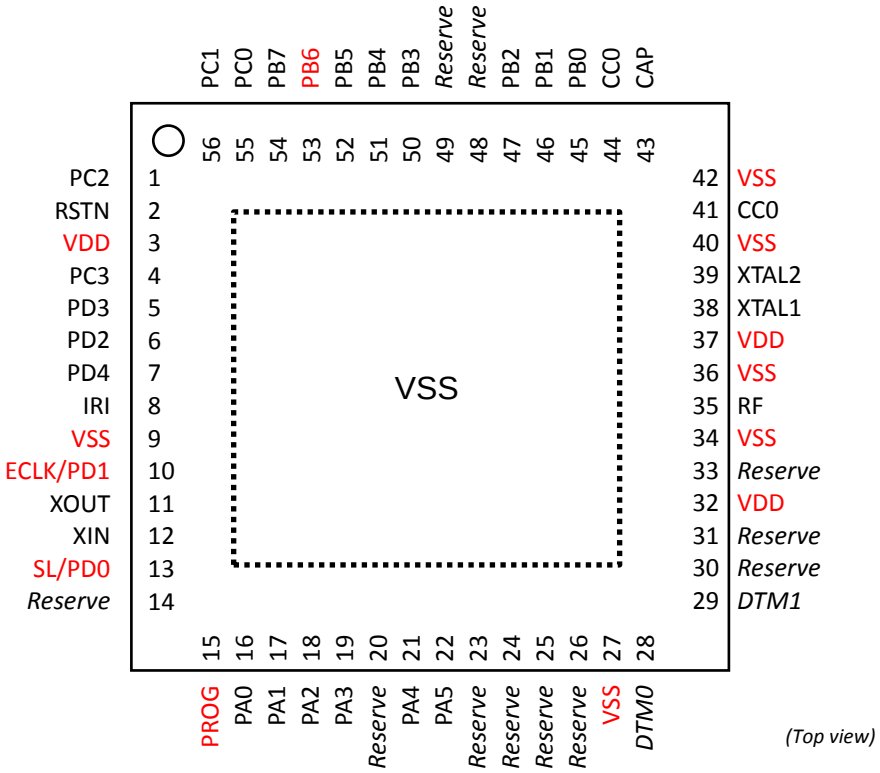
DC6688BT32UL

(QFN32)



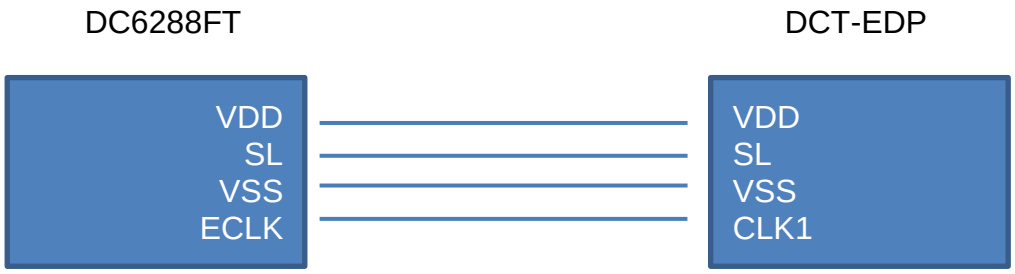
DC6688BT96UZ

(QFN56)

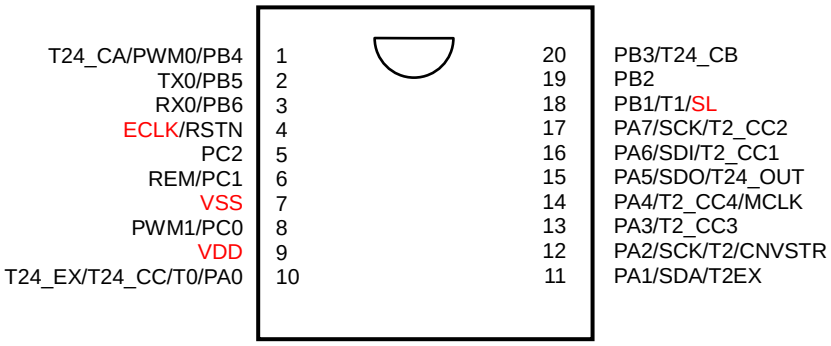


4.5 DC6288FT

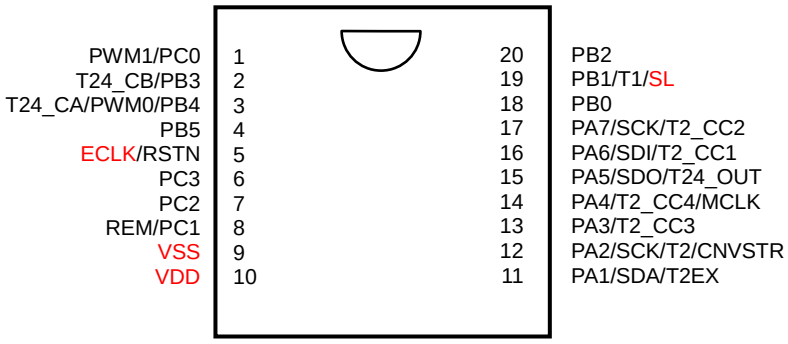
To do trimming during programming stage, 4 pads are required on PCB to complete this process.



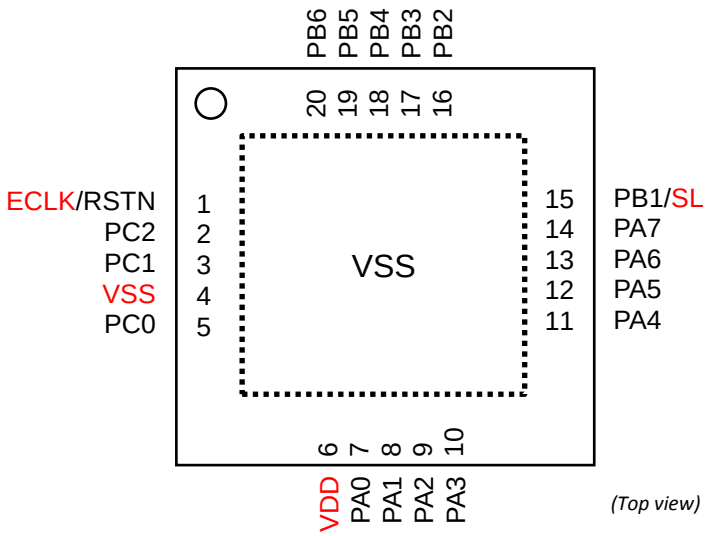
TSSOP20-M



TSSOP20-R

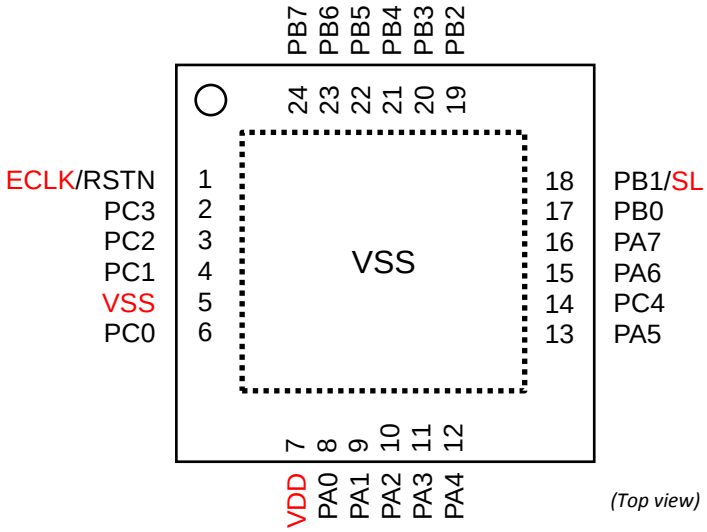


(QFN20)



(Top view)

(QFN24)


PB7 PB6 PB5 PB4 PB3 PB2
24 23 22 21 20 19
ECLK/RSTN 1
PC3 2
PC2 3
PC1 4
VSS 5
PC0 6
VSS
18 PB1/SL
17 PB0
16 PA7
15 PA6
14 PC4
13 PA5
7 8 9 10 11 12
VDD PA0 PA1 PA2 PA3 PA4
(Top view)

Revision History

Document Rev. No.	Issued Date	Section	Page	Description	Edited By	Reviewed By
1.0	May, 2019	All	-	Preliminary	Danny Ho	Patrick Li
1.1	May, 2019	5		Add section 5 for programming	Danny Ho	Patrick Li
		2.5		Add section for pin assignment		
1.2	June, 2019	6.1		Add 'hardware setup'	Danny Ho	Patrick Li
		3		Add 'Debug'		
1.3	June, 2019	All		Re-organize the content Added section 3.3.2	Danny Ho	Patrick Li

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